

FORM PT01449 (REV. 8-83)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. HARI.006USM		SERIAL NO. 09/064,250								
INFORMATION DISCLOSURE STATEMENT <i>(Use several sheets if necessary)</i>				APPLICANT HARARI et al.										
				FILED April 22, 1998		GROUP 2785								
U. S. PATENT DOCUMENTS														
*EXAMINER INITIAL	A1	3	6	3	3	1	7	5	DATE	NAME	CLASS	SUB CLASS	FILING DATE	
Ju	A1	3	6	3	3	1	7	5	1/4/72	Harper	340	172.5		
Ju	A2	4	2	7	9	0	2	4	7/14/81	Schrenk	365	203		
Ju	A3	4	3	5	5	3	7	6	10/19/82	Gould	365	209	998	
Ju	A4	4	6	1	6	3	1	1	10/7/86	Sato	369	200		
Ju	A5	4	6	5	4	8	4	7	3/31/87	Dutton	371	2700		
Ju	A6	4	7	3	3	3	9	4	3/22/88	Giebel	371	21		
Ju	A7	4	9	4	5	5	3	5	7/31/90	Hosotani et al.	371	11.1		
Ju	A8	5	0	5	1	8	8	7	9/24/91	Berger et al.	364	200		
Ju	A9	5	0	9	5	3	4	4	3/10/92	Harari	357	23.5		
Ju	A10	5	1	6	3	0	2	1	11/10/92	Mehrotra et al.	365	185		
Ju	A11	5	1	7	2	3	3	8	12/15/92	Mehrotra et al.	365	185		
FOREIGN PATENT DOCUMENTS														
		DOCUMENT NUMBER							DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)	
Ju	B1	JP	62	2	8	3	4	9	6	12/1987	Japan	—	—	Yes
Ju	B2	GB	2	1	3	6	9	9	2	09/1984	United Kingdom	—	—	
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)														
Ju	C1	Torelli et al., "An Improved Method for Programming a Word-Erasable EEPROM", Alta Frequenza, Vol. 52, Nov. - Dec. 1983, no. 6, pp. 487-494.												
EXAMINER Vule										DATE CONSIDERED 10/29/04				
* EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.														

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U.S. Department of Commerce, Patent and Trademark Office	Atty. Docket No.	Application No.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	SNDK.006USM	09/064,250
(Use several sheets if necessary)	Applicant(s)	Conf. No.
(Form PTO-1449)	HARARI et al.	5711
	Filing Date	Group
	April 22, 1998	2824

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*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	4,090,258	05-1978	Cricchi			
	4,149,270	04-1979	Cricchi et al.			
	4,181,980	01-1980	McCoy			
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	4,253,059	02-1981	Bell et al.			
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	DE3637682	05/1987	Germany				abstract	
	DE3831538	03/1989	Germany				abstract	
	GB2061651	05/1981	United Kingdom					
	GB2029145	03/1980	United Kingdom					

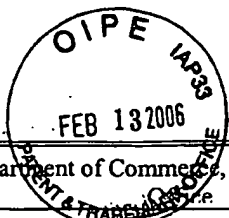
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	Alberts et al., "Multi-Bit Storage Fet Earom Cell", IBM Technical Disclosure Bulletin, Vol. 24, No.7A, Dec. 1981, pp. 3311-3314, 4193.
	Berenga et al. "E2-PROM TV Synthesizer", 1978 IEEE International Solid-State Circuits Conference: ISCCC 78", February 17, 1978, pp.196-197.
	"Bipolar /MOS Memories Data Book", <u>Advanced Micro Devices</u> , ISSN 0888-4714, pp.6-1-6-14, 1986
	Bleiker et al., "A Four State EEPROM Using Floating-Gate Memory Cells", IEEE Journal of Solid-State Circuits, Vol. Sc-22. No. 3, June 1987, pp.460-463.

Examiner /Vu Le/ Date Considered 01/30/2008

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /V.L./



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	4,685,082	08-1987	Cheung			
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	4,779,272	10-1988	Kohda et al.			
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	4,809,231	02-1989	Shannon et al.			
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	JP62188100	08/1987	Japan				abstract	
	JP0123878	05/1989	Japan					X
	JP0146949	10/1989	Japan					X

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	Caironi et al., "A TV Frequency Synthesis System With a Single Chip Microprocessor Interface Including Non-Volatile Memory", IEEE Transactions on Consumer Electronics", Vol. CE-28, No.3, pp.363-71, August 1982.
	Furuyama et al., "An Experimental 2-BIT/CELL Storage Dram for Macro Cell or Memory-on-Logic Application", IEEE Custom Integrated Circuits Conference, May 1988, pp. 4.4.1-4.4.4.
	Gee et al., "An Enhanced 16K E2PROM", IEEE Journal of Solid-State Circuits, Vol. SC-17, No.5, October 1982, pp. 828-832.
	Horiguchi et al. "An Experimental Large-Capacity Semiconductor File Memory Using 16-LEVEL/CELL storage", IEEE Journal of Solid-State Circuits, Vol. 23, Feb.1998, No.1, pp. 27-33.

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				Filing Date		Group		
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	59	6,263,003	Nov. 16, 1993	Cowles et al.				
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							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
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	61	DE2840305	1989	Germany	03/1980		Abstract	
	62	EP0086886	08/1983	EPO				
	63	EP0220718	05/1987	EPO				
	64	EP0300264	01/1989	EPO				
	65	EP0392895	10/1990	EPO				
	66	EP0243503	11/1989	EPO				
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	69	EP0569040	11/1993	EPO				
	70	EP0615193	07/1994	EPO				
	71	GB2136992	09/1984	United Kingdom				
	72	GB2251323	07/1992	United Kingdom				
	73	GB2251324	07/1992	United Kingdom				
	74	60178564	09/1985	Japan			Abstract	
Examiner		/Vu Le/		Date Considered		09/10/2008		
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Foreign Patent Documents								
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		Document	Date	Country	Class	Subclass	Yes	No
	75	60179857	04/1985	Japan			Abstract	
	76	1235075	09/1989	Japan			Abstract	
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	91	DE3200872	07/1983	Germany			Abstract	
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	92	Jex "Flash Memory BIOS for PC and Notebook Computers", 1991, IEEE, pp. 692-695.						
	93	Wilson, "1-Mbit Flash Memories Seek their role in System Design", Computer Design, vol. 28, no. 5, pp. 30 and 32, March 1989.						
	94	Bonner, "Flash Memory for Top Speeds in Mobile Computing Applications", Computer Technology Review, vol. 12, no. 7, June 1992, pp. 36-37.						
	95	Williams, "Asymmetric Memory Hierarchies", Communications of the Association for Computing Machinery, vol. 16, no. 4, April 1973, pp. 213-222.						
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